MAXIM

Complete 5μs CMOS 10-Bit A/D Converter

MAX173

General Description

The MAX173 is a complete, 10-bit linear analog-to-digital converter (ADC) that combines high speed, low power consumption, and an on-chip voltage reference. The conversion time is 5μs. The buried zener reference provides low drift and low noise performance.

External component requirements are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry is also included which can either be driven from an external source, or in stand-alone applications, from a crystal.

The MAX173 uses a standard microprocessor interface architecture. Three-state data outputs are controlled by Read (RD) and Chip Select (CS) inputs. Data access and bus release times of 90ns and 75ns respectively ensure compatibility with most popular microprocessors without resorting to wait states.

Applications

Digital Signal Processing (DSP)

High Accuracy Process Control

High Speed Data Acquisition

Electro-Mechanical Systems

Features

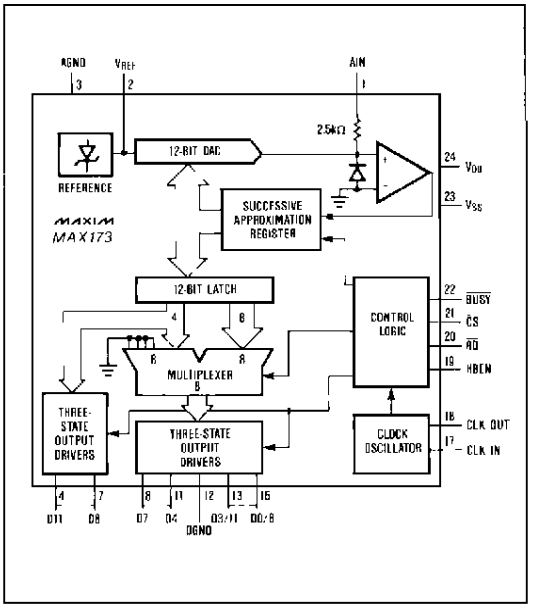
- **12-Bit Resolution and 10-Bit Linearity**
- **5μs Conversion Time**
- **On-Chip ±40ppm/°C Voltage Reference**
- **90ns Access Time**
- **215mW (Max) Power Consumption**
- **24-Lead Narrow DIP and Wide SO Packages**

Ordering Information

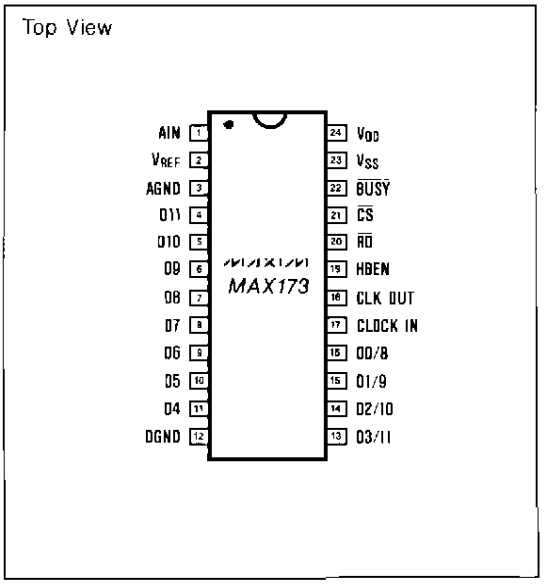
PART	TEMP. RANGE	PACKAGE*
MAX173CNG	0°C to +70°C	Plastic DIP
MAX173CWG	0°C to +70°C	Wide SO
MAX173C/D	0°C to +70°C	Dice**
MAX173ENG	-40°C to +85°C	Plastic DIP
MAX173EWG	-40°C to +85°C	Wide SO
MAX173MRG	-55°C to +125°C	CERDIP

* All devices — 24 lead packages
** Consult factory for dice specifications

Functional Diagram



Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V, V_{DD} + 0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V, V_{DD} + 0.3V
(Pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX173XC ..... 0°C to +70°C
MAX173XE ..... -40°C to +85°C
MAX173XM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) to +75°C 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ± 5%, V_{SS} = -12V or -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 2.5MHz.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
No Missing Code Resolution				10			Bits
Integral Non-Linearity	INL					±0.05	%FSR
Offset Error (Note 1)						±5	mV
Full Scale Error (Note 2)						±0.4	%
Full Scale Tempco (Notes 3, 4)						±45	ppm/°C
ANALOG INPUT							
Input Voltage Range				0		5	V
Input Current		AIN = 0V to +5V				3.5	mA
INTERNAL REFERENCE							
V_{REF} Output Voltage		T_A = 25°C		-5.2	-5.25	-5.3	V
V_{REF} Output Tempco (Note 5)					±40		ppm/°C
Output Current Sink Capability		(Note 6)				5	mA
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, RD, HBEN, CLKIN				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, RD, HBEN, CLKIN		2.4			V
Input Capacitance (Note 7)	C_{IN}	$\overline{CS}$ $\overline{RD}$, HBEN, CLKIN				10	pF
Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN CLKIN	VIN = 0 to V_{DD}			±10 ±20	µA
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SINK} = 1.6 mA				0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLKOUT I_{SOURCE} = 200µA		4			V
Floating State Leakage Current	I_{LKG}	D11-D0/8, V_{OUT} = 0V to V_{DD}				±10	µA
Floating State Output Capacitance (Note 7)	C_{OUT}					15	pF
CONVERSION TIME							
MAX173	t_{CONV}	Synchronous (12.5 clock cycles) Asynchronous (12 to 13 clock cycles)		 4.8		5 5.2	µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ± 5%, V_{SS} = -12V or -15V ± 5%; Slow Memory Mode; T_A = T_{MIN} to T_{MAX} unless otherwise noted, f_{CLK} = 2.5MHz.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REJECTION						
V_{DD} Only		FS Change, V_{SS} = -15V, V_{DD} = 4.75V to 5.25V		+0.01		%
V_{SS} Only		FS Change, V_{DD} = 5V, V_{SS} = -5% to +5%		+0.01		%
POWER REQUIREMENTS						
V_{DD}		+5% for Specified Performance		5		V
V_{SS} (Note 8)		±5% for Specified Performance		-12 or -15		V
I_{DD}		$\overline{CS}$ $\overline{RD}$ = V_{DD}, AIN = 5V		5	7	mA
I_{SS}		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN 5V		8	12	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -15V		145	215	mW

Note 1: Typical change over temp is ±1.2mV.
Note 2: V_{DD} = +5V, V_{SS} = -15V, FS +5.000V. Ideal last code transition = FS - 1.8mV.
Note 3: Full Scale TC = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Includes internal reference drift.
Note 5: V_{REF} TC = $\Delta V_{REF}/\Delta T$, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}
Note 6: Output current should not change during conversion.
Note 7: Guaranteed by design, not subject to test.
Note 8: Functional operation at V_{SS} = -12V ± 5% is guaranteed by testing offset error and full scale error

TIMING CHARACTERISTICS (Note 9) (See MAX162 data sheet for t_1-t_{10} description)

(V_{DD} +5V, V_{SS} = -12V or -15V; T_A = T_{MIN} to T_{MAX}, specifications in bold type are 100% tested, others are guaranteed by design, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C			MAX173C/E		MAX173M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay (Note 12)	t_2	C_L = 50pF		**90**	**190**		**230**		**270**	ns
Data Access Time (Note 10)	t_3	C_L = 20pF		60	90		110		120	ns
Data Access Time (Notes 10, 12)	t_3	C_L = 100pF		70	**125**		**150**		**170**	ns
$\overline{RD}$ Pulse Width	t_4		t_3			t_3		t_3		
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ (Notes 10, 12)	t_6				**80**		**105**		**120**	ns
Bus Relinquish Time (Notes 11, 12)	t_7				**75**		**85**		**90**	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between Read Operations	t_{10}		200			200		200		ns

Note 9: All input control signals are specified with t_f = t_r = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 10: t_3 and t_6 are measured with the load circuits of Figure 1 (see MAX162 data sheet) and defined as the time required for an output to cross 0.8V or 2.4V.
Note 11: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2 (see MAX162 data sheet).
Note 12: This specification is 100% production tested.

For additional information on using the MAX173 please refer to MAX162 data sheet.

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Chip Topography